Amendments to the Specification

Please replace the paragraph beginning at page 14, line 1, with the following rewritten paragraph:

Figure 2 is a block diagram illustration of memory error management computer system 200, one exemplary system for implementing methods of the present invention. Memory error management computer system 200 comprises a host 210 and memory device 250. In one embodiment of the present invention memory device 250 is a peripheral or an auxiliary memory device (e.g., a disk array storage system). Memory device 250 includes physical memory medium 240 (e.g., a disk array subsystem), a first memory controller 220 and a second memory controller 230. Memory controller 220 and memory controller 230 include memory controller buffers 221 and 231 respectively. In one embodiment of the present invention, memory controller buffers 221 and 223. are caches. As indicated schematically by bus lines 270, ~~Host~~ host 210 is coupled to memory controllers 221 and 231 which are coupled to physical memory medium 240. In one exemplary implementation of the present invention, host 210 is a server computer system that provides access and services to other computers (not shown).